LCC MODULE REFERENCE DESIGN

REVISION HISTORY

REVISION	DATA	DESCRIPTION
V1.0	2017/04/01	INITIAL RELEASE
V1.1	2017/04/11	SHEET 2 ADD ME3612 DESIGN ATTENTION
V1.2	2018/02/08	CHANGE C24/C2/C55/C19/C3/C54/C20/C17/C7/C16 TO 33PF
V1.3	2018/04/12	OPTIMIZE THE MATCHING CIRCUIT OF MAIN_ANT/AUX_ANT/GNSS_ANT

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SIZE A4+

ME3630 DESIGN ATTENTION

1	DO NOT PULL UP PIN 7/8/60/77
2	DO NOT USE PIN 19 AS INPUT

ME3612 DESIGN ATTENTION

1	DO NOT PULL UP PIN 7/8/64/77

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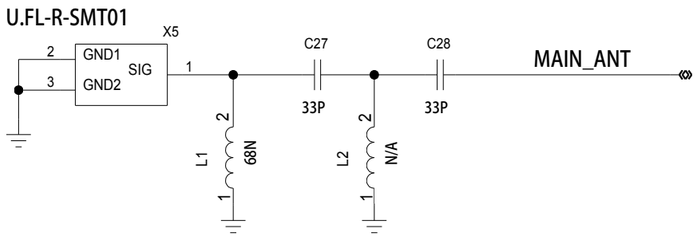
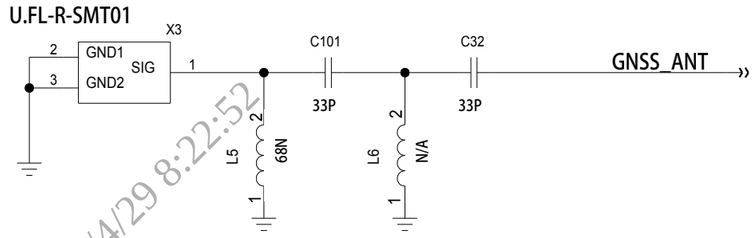
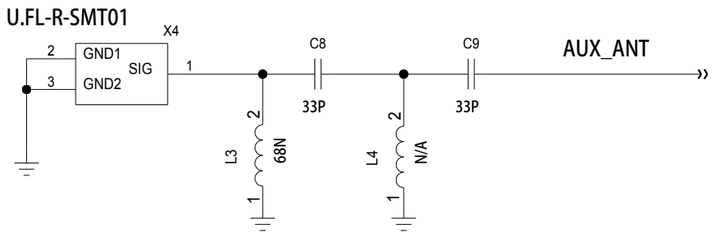
SIZE A4+

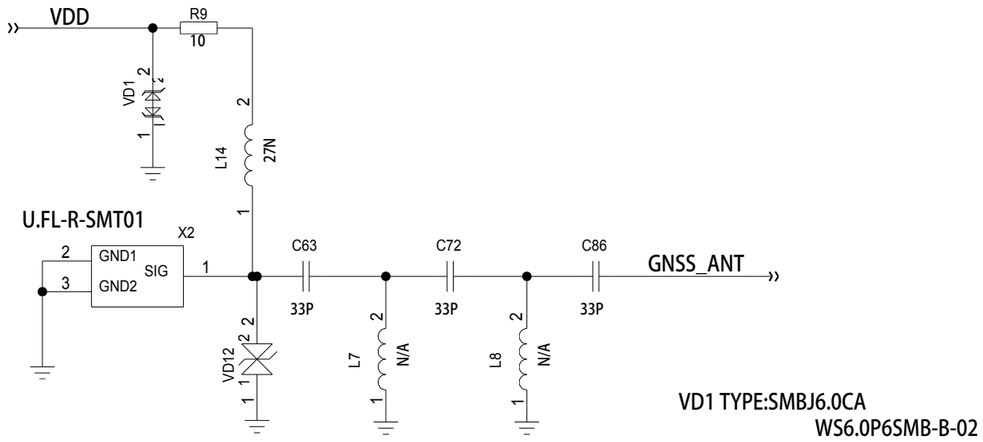
RF REF DESIGN





GNSS PASSIVE ANTENNA





VD1 TYPE:SMBJ6.0CA
WS6.0P6SMB-B-02
VD12 TYPE:ESD03C32D-LCD

GNSS ACTIVE ANTENNA

NOTES:
VDD IS POWER SUPPLY FOR ANTENNA,
PLEASE ACCORDING TO THE SELECTED ANTENNA REQUIREMENTS FOR POWER SUPPLY DESIGN.

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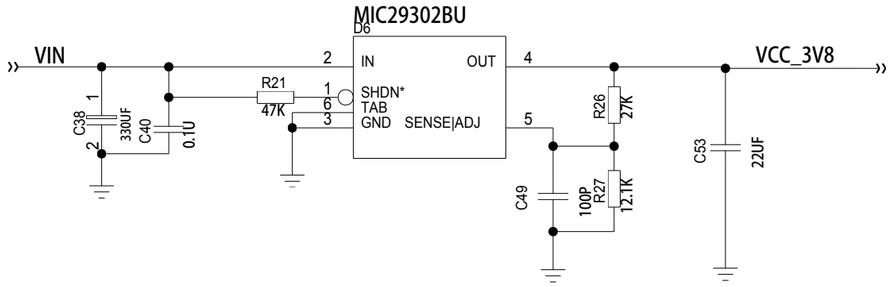
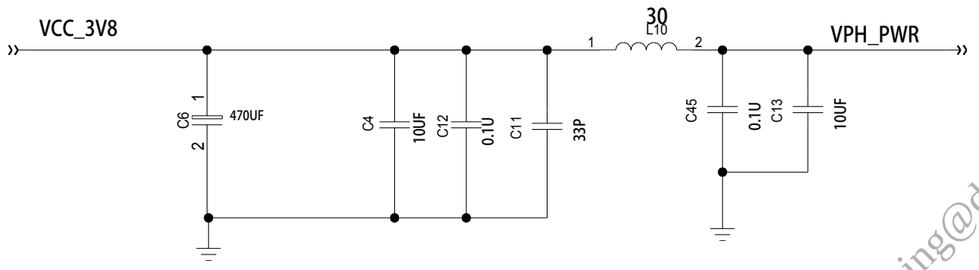
LDO REF DESIGN



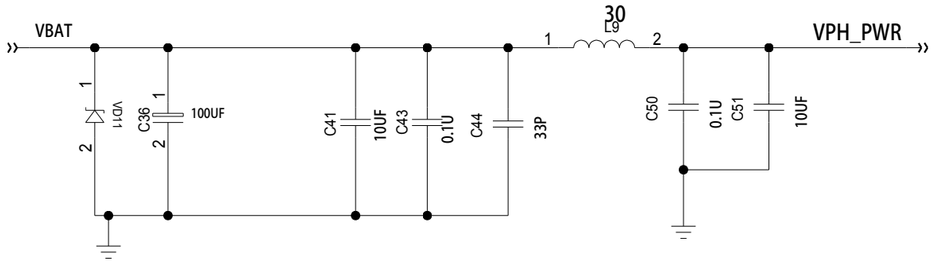
FB: 1.24V
VIN:16V 3A

D6 TYPE:MIC29302WU
XRP29302ETBTR-L



PLACE CLOSE TO MODULE

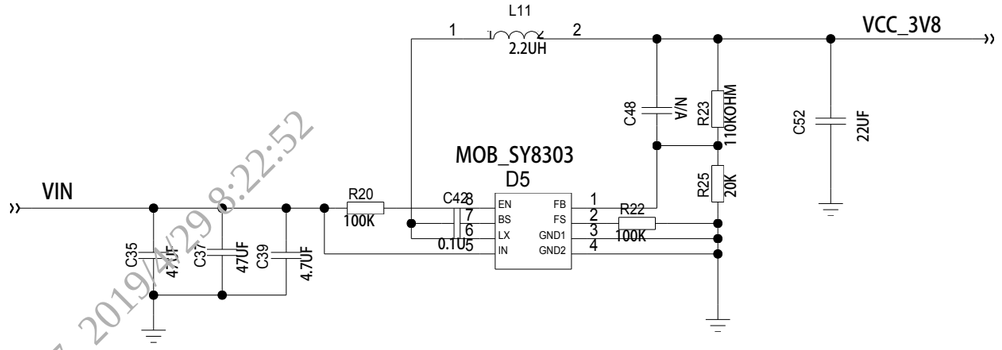
VBAT SUPPLY



VD11 TYPE:MMSZ5231BS-7-F
MM3Z5V1T1G

DCDC REF DESIGN

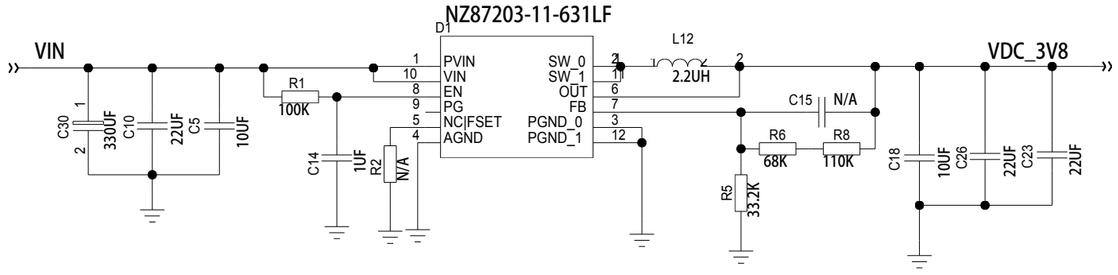
1



FB: 0.6V
VIN:4.5V-40V 3.0A

D5 TYPE:SY8303AIC

2



FB: 0.6V
VIN: 2.7V-6V 3.5A

D1 TYPE:NZ87203-11-631LF
PAM2326AGPADJ

DRAWING

LAST_MODIFIED=Thu Apr 12 09:39:29 2018

SIZE:A4+

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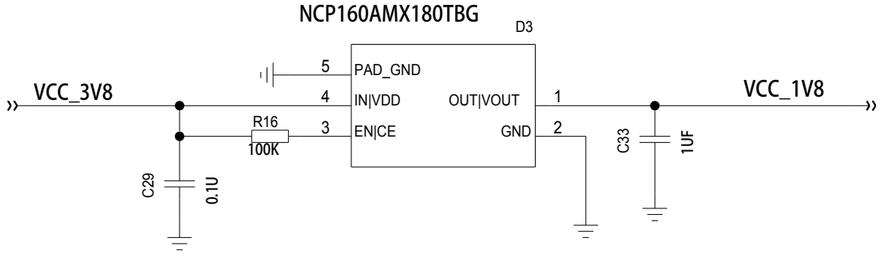
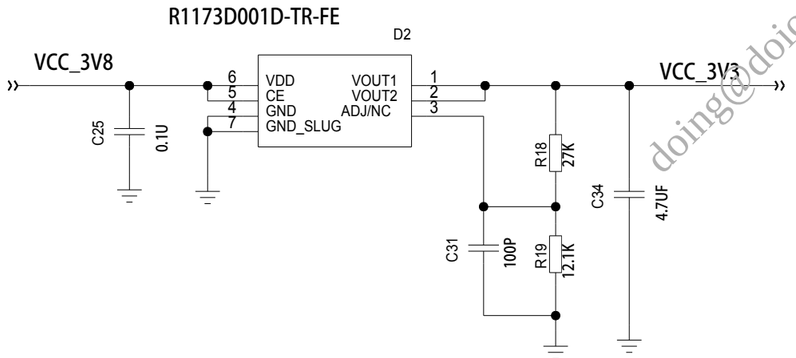
TITLE: LCC MODULE REFERENCE DESIGN	VERSION:	V1.1

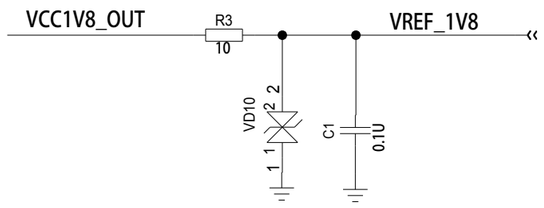
1.8V OUT



3.3V OUT



MODULE'S 1V8 OUT



VD10 TYPE:ESDHB5V0AE1
VESD54151

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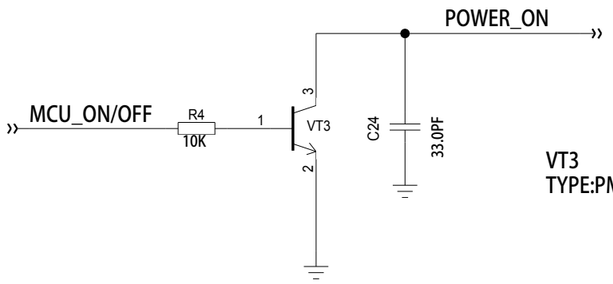
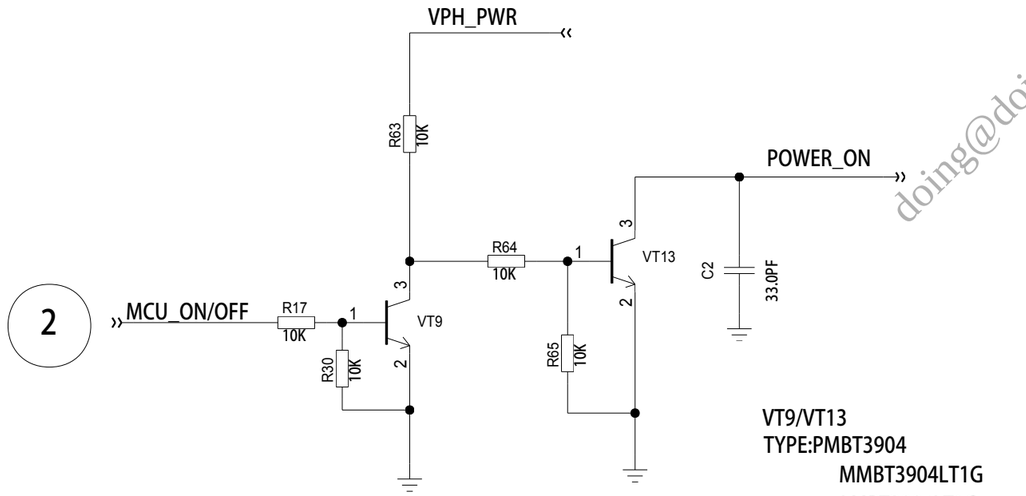
SIZEA4+

POWERON REF DESIGN



VT3
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

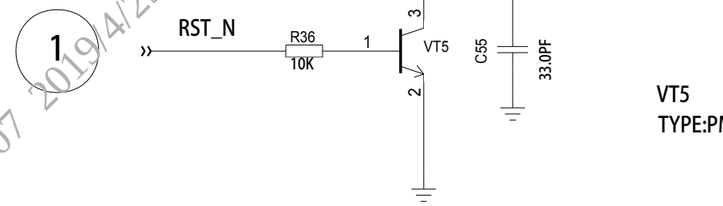
PULL ON/OFF HIGH TO POWER ON



VT9/VT13
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

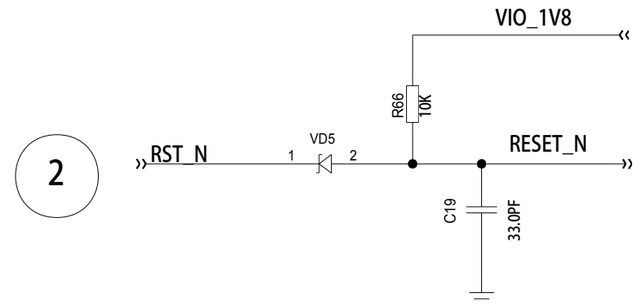
PULL ON/OFF LOW TO POWER ON

RESET REF DESIGN



VT5
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

PULL RST_N HIGH TO RESET



VD5
TYPE:RB551VM-30TE-17
B0530WS-7-F

PULL RST_N LOW TO RESET

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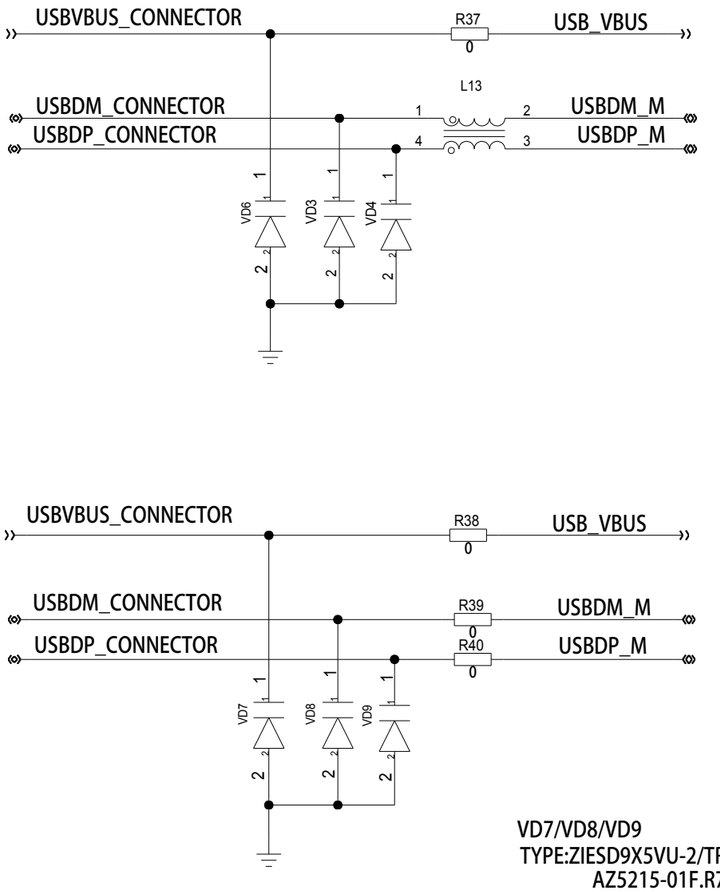
SIZE:A4+

USB REF DESIGN

FOR USB CONNECTOR

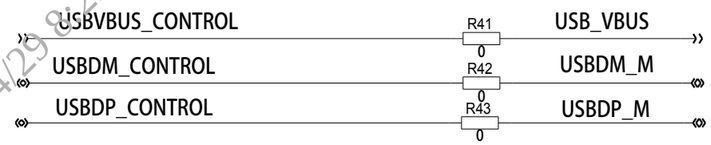


VD6/VD3/VD4
TYPE:ZIESD9X5VU-2/TR
AZ5215-01F.R7GZ

L5
TYPE:DLM0NSN900HY2D
EXC14CT900U
MCF08062G900-T

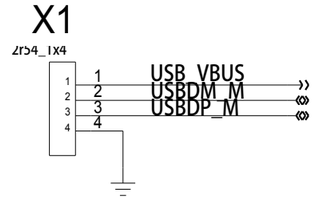
VD7/VD8/VD9
TYPE:ZIESD9X5VU-2/TR
AZ5215-01F.R7GZ

FOR MCU CONTROLER



FOR USB NC:

SHOULD ADD TEST POINTS FOR DEBUG



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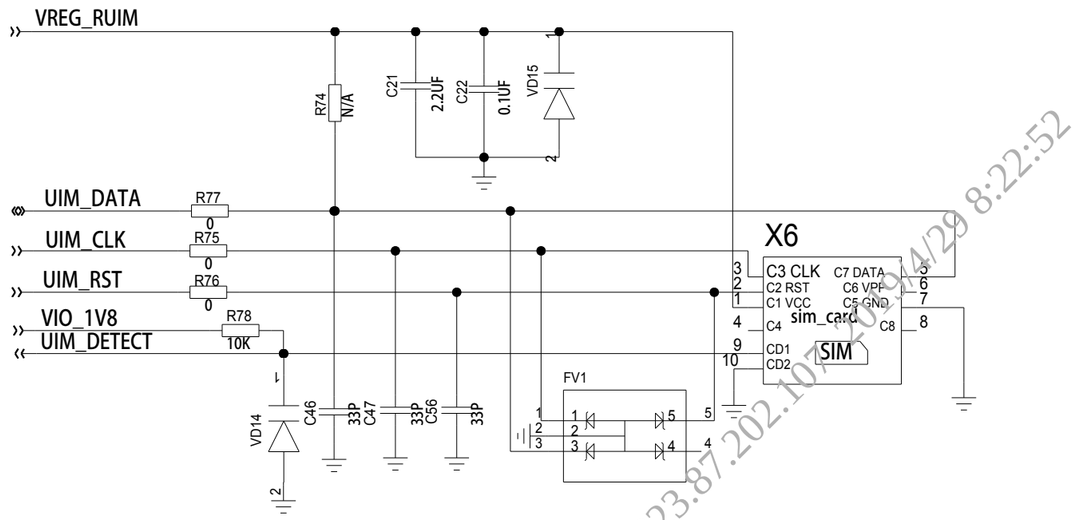
SIM REF DESIGN



NOTES:

1.FOR ME3620,R74 SHOULD BE 10K OHM.
FOR ME3630,R74 CAN BE NA, UIM_DATA PULL-UP HAS BEEN ADDED IN MODULE.

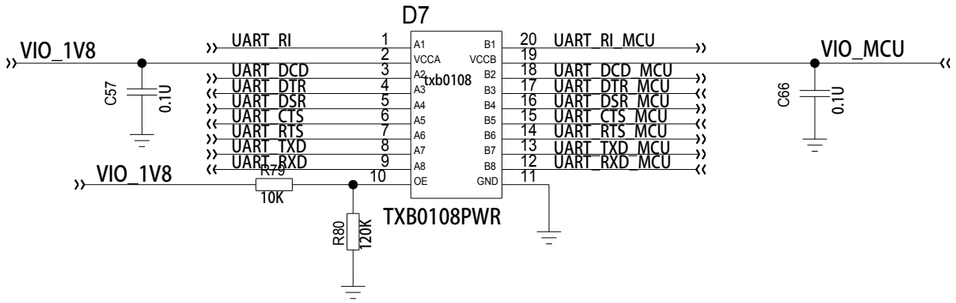
2.RECOMMENDED ADD AN ESD PROTECTION DEVICE FOR SIM PROTECTION.
PLEASE PLACE ESD NEAR THE SIM CARD AND LAYOUT FIRST THROUGH ESD DEVICE.

3.RECOMMENDED ADD 33PF BETWEEN UIM_CLK, UIM_DATA, UIM_RST AND GND TO FILTER RF SIGNAL INTERFERENCE.

4.RECOMMENDED ADD SERIES RESISTANCE IN UIM_DATA AND UIM_CLK SIGNAL.

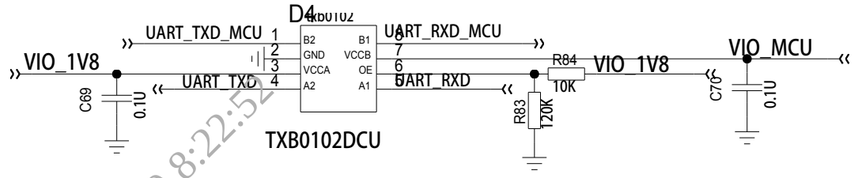
5.UIM_DETECT IS THE INPUT SIGNAL OF THE MODULE, 1.8V.
RECOMMENDED PUII UP UIM_DETECT TO THE REFERENCE LEVEL (1.8V) BY 10K.
IT IS USED TO DETECT SIM CARD.
WHEN IT IS LOW, THERE IS A CARD, FOR HIGH, NO CARD.
PLEASE CONFIRM IF THE SIM CONNECTOR PLUG MEET THE HARDWARE REQUIREMENTS.

UART LEVER TRANSLATOR



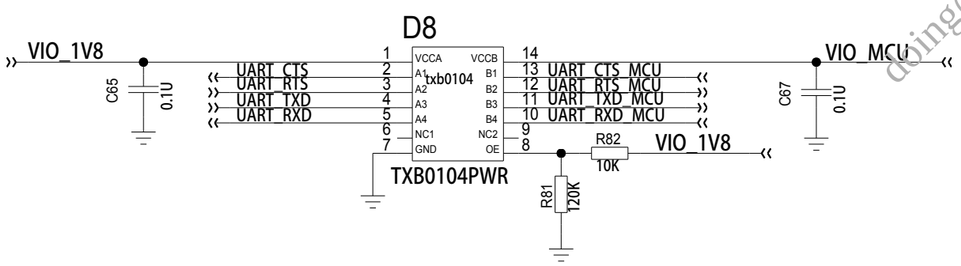
NOTES:

1.THE VOLTAGE DOMAIN OF UART IS 1.8V.
TXB0108 REALIZE THE VOLTAGE LEVEL TRANSLATION BETWEEN MODULE AND MCU.
2.VCCA SHOULD NOT EXCEED VCCB.
3.FOR MORE INFORMATION ABOUT TXB0108, PLEASE REFER TO THE DATASHEET.



NOTES:

1.THE VOLTAGE DOMAIN OF UART IS 1.8V.
TXB0102 REALIZE THE VOLTAGE LEVEL TRANSLATION BETWEEN MODULE AND MCU.
2.VCCA SHOULD NOT EXCEED VCCB.
3.FOR MORE INFORMATION ABOUT TXB0102, PLEASE REFER TO THE DATASHEET.



NOTES:

1.THE VOLTAGE DOMAIN OF UART IS 1.8V.
TXB0104 REALIZE THE VOLTAGE LEVEL TRANSLATION BETWEEN MODULE AND MCU.
2.VCCA SHOULD NOT EXCEED VCCB.
3.FOR MORE INFORMATION ABOUT TXB0104, PLEASE REFER TO THE DATASHEET.

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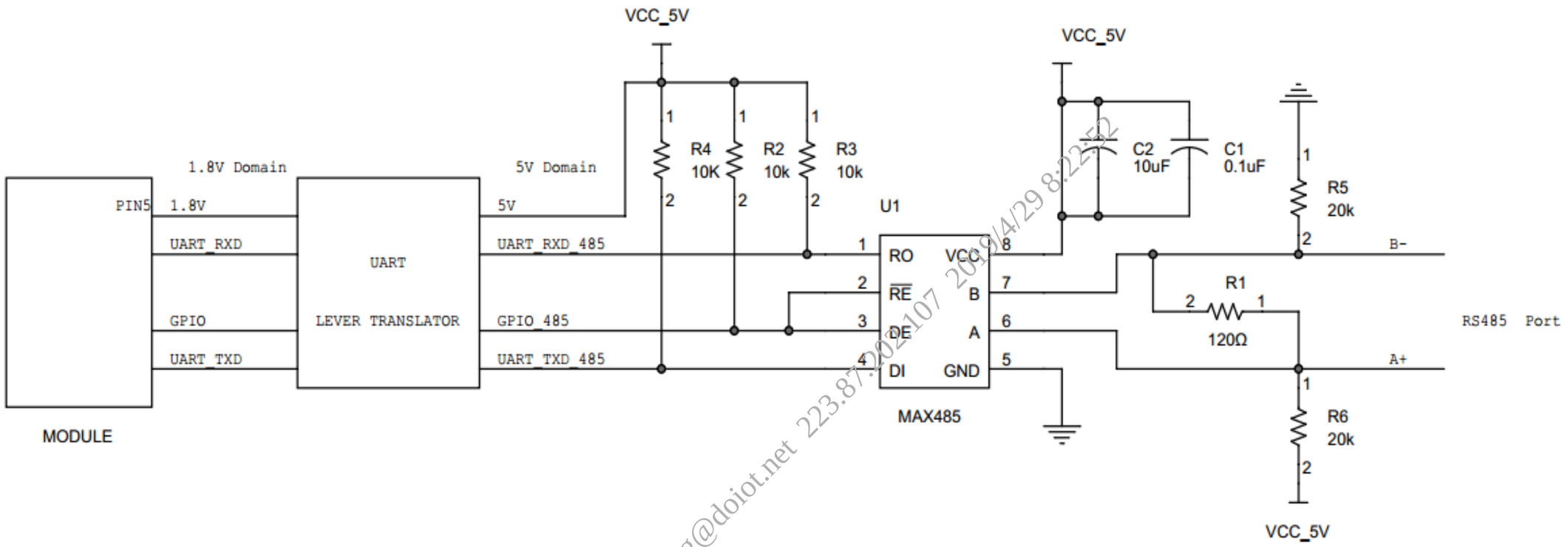
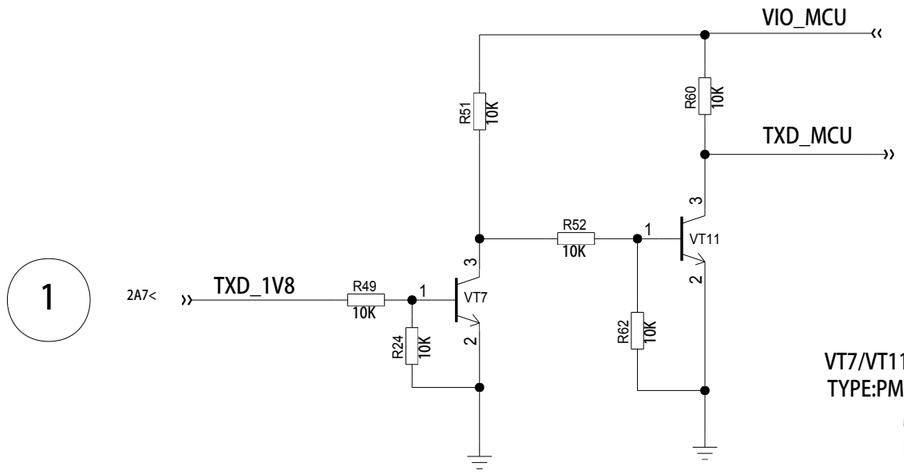
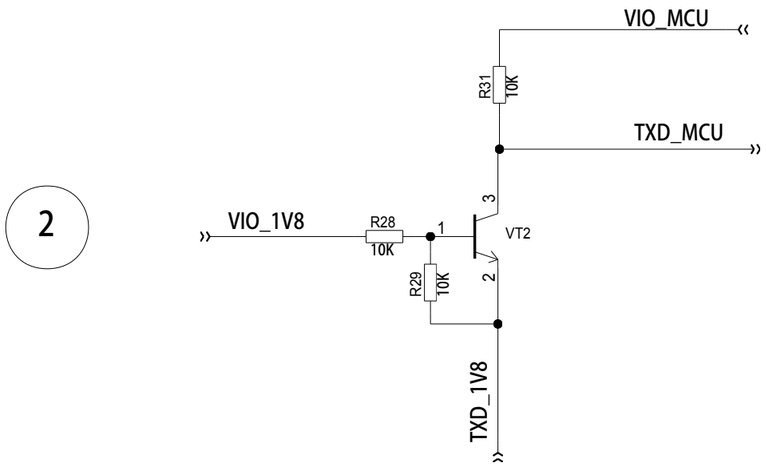


If use the 485 circuit, the program should be custom-made

UART_TX REF DESIGN

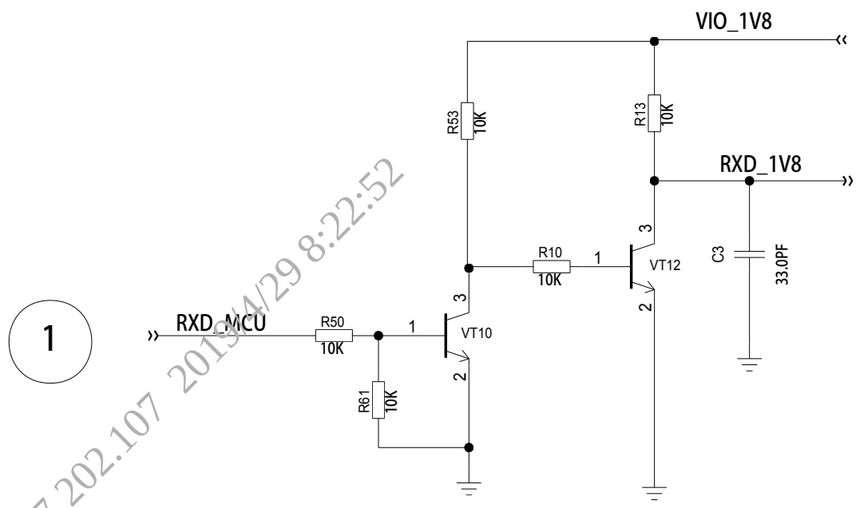


VT7/VT11
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G



VT2
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

UART_RX REF DESIGN



VT10/VT12
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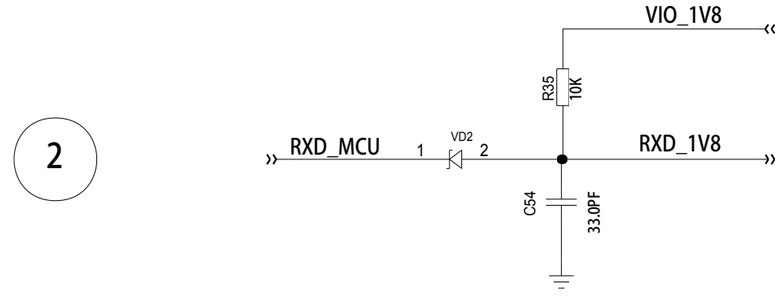
MMBT3904LT1G
LMBT3904LT1G



VD2 TYPE:RB551VM-30TE-17
B0530WS-7-F

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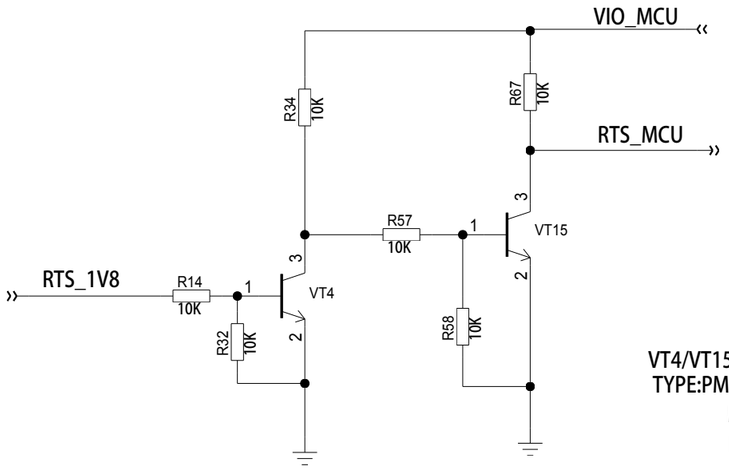
SIZEA4+

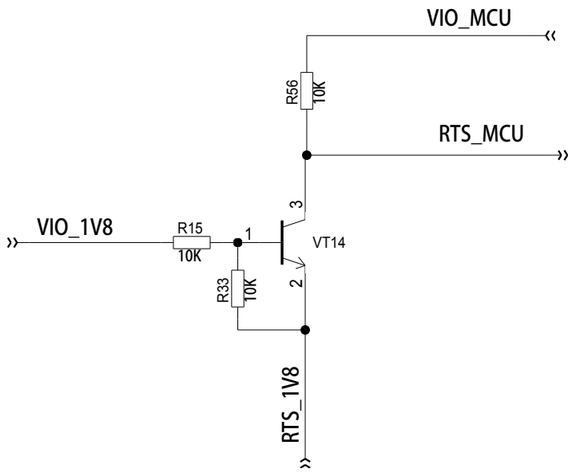
UART_RTS REF DESIGN

1



VT4/VT15
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

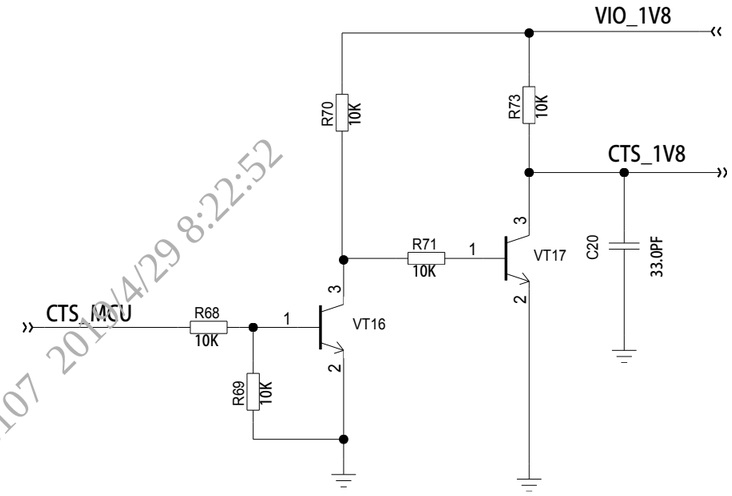
2



VT14
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

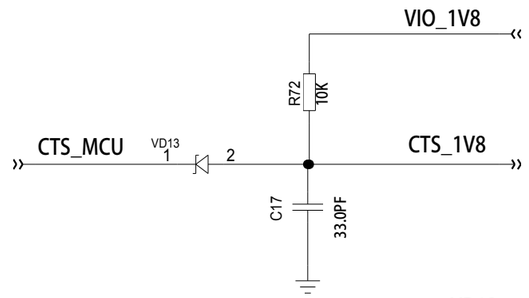
UART_CTS REF DESIGN

1



VT16/VT17
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

2



VD13
TYPE:RB551VM-30TE-17
B0530WS-7-F

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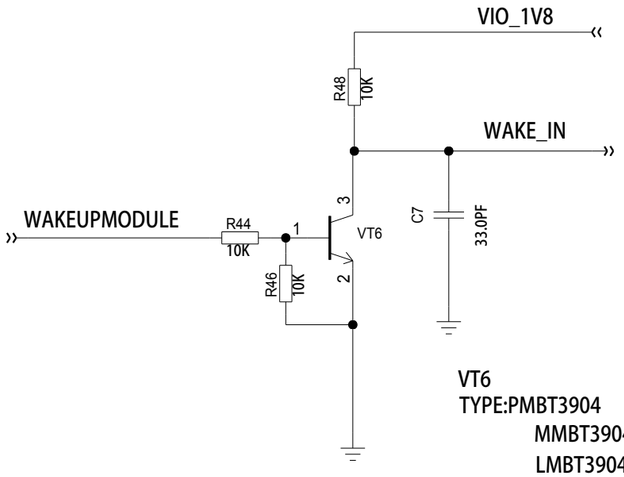
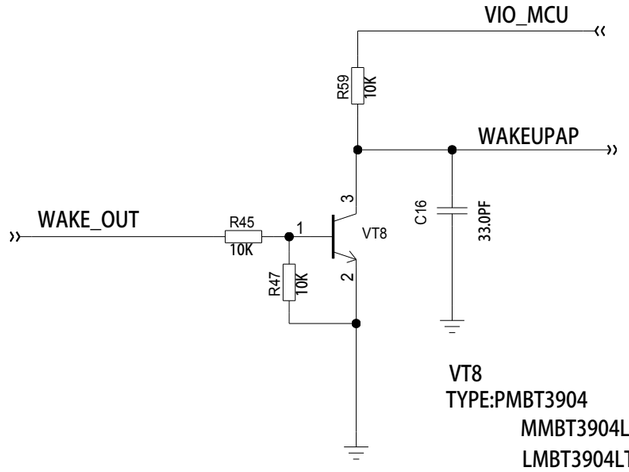
SIZE:A4+

WAKE_IN REF DESIGN



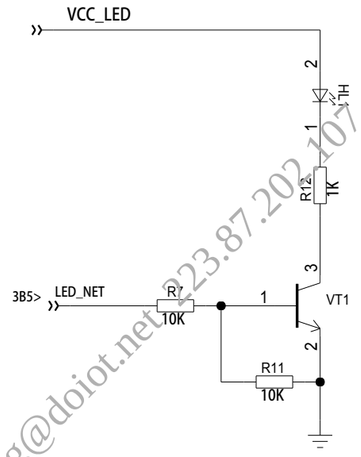
VT6
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

WAKE OUT REF DESIGN



VT8
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

LED REF DESIGN



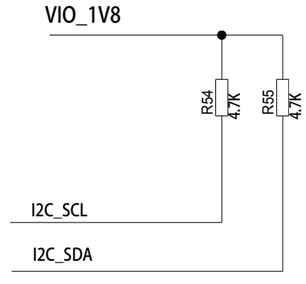
VT1
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

NOTES:

BEFORE DESIGN,PLEASE CHECK IF LED_NET IS A GPIO.
IF IT IS,ITS DESIGN CAN REFER THIS SCH.
IF IT IS NOT,IT CAN NOT USE THIS REF DESIGN.

DEBUG UART(PIN67/68) SHOULD ADD TEST POINTS FOR DEBUG.

I2C REF DESIGN



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